

DRAWING(S)

Figs. 1-15 are attached as formal drawings.

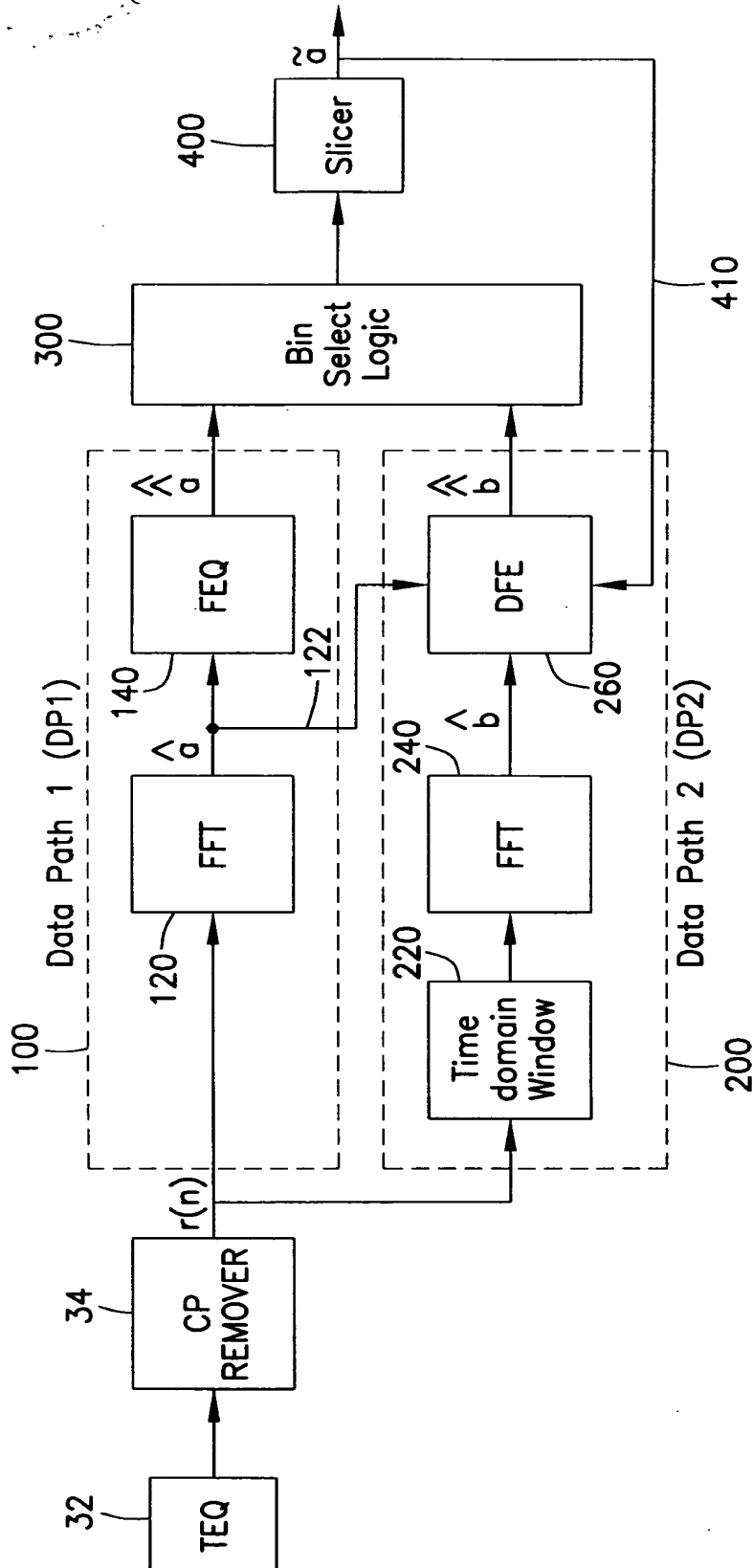


Fig. 1

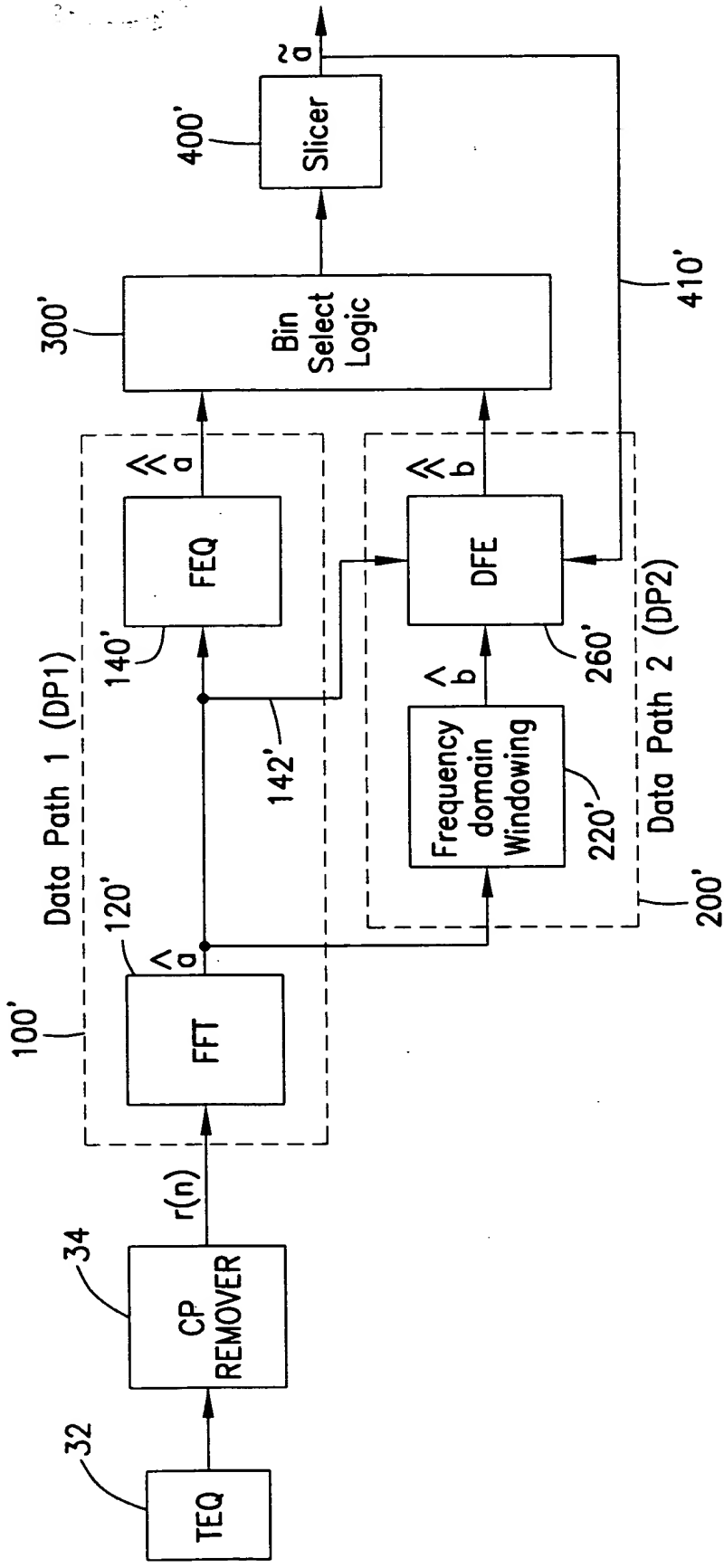


Fig. 2

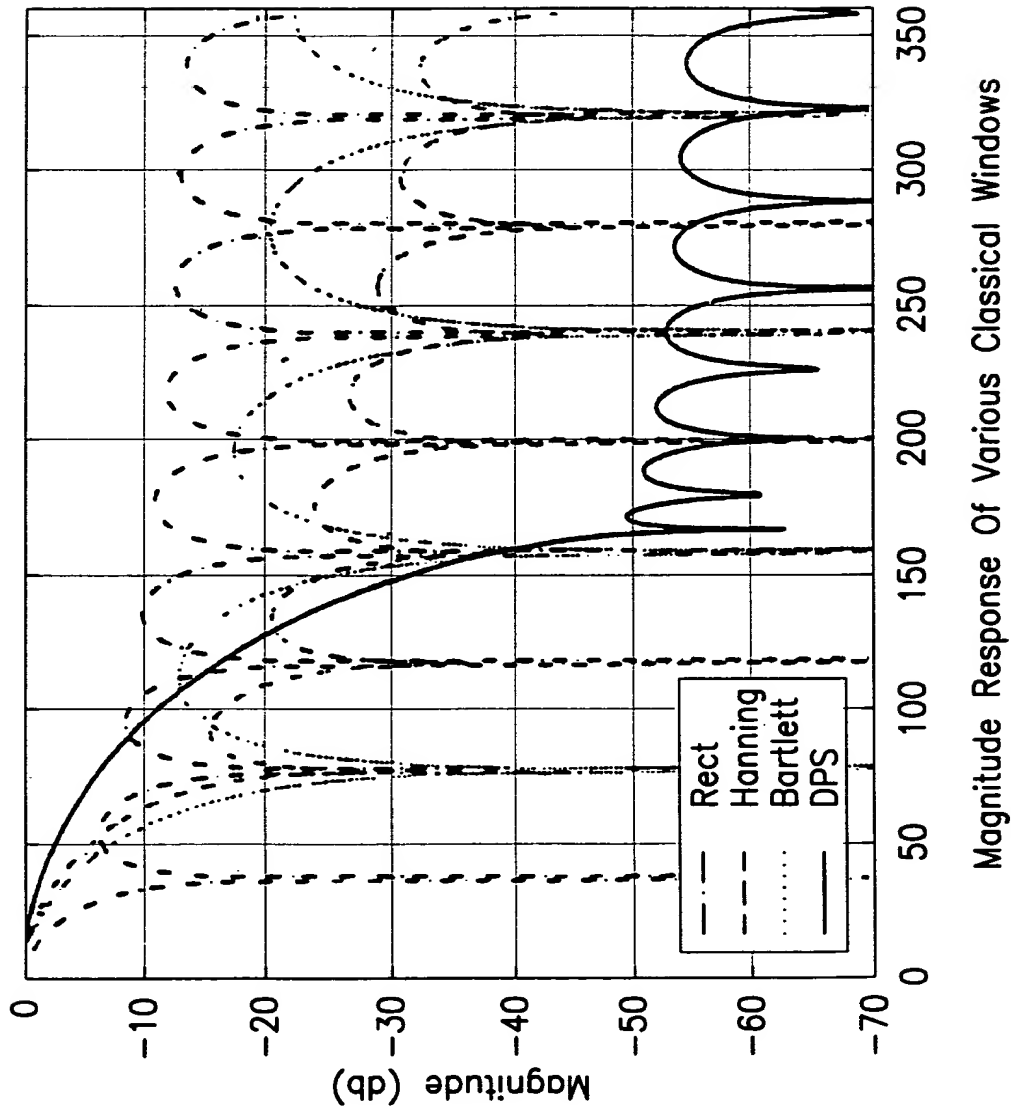


Fig. 3

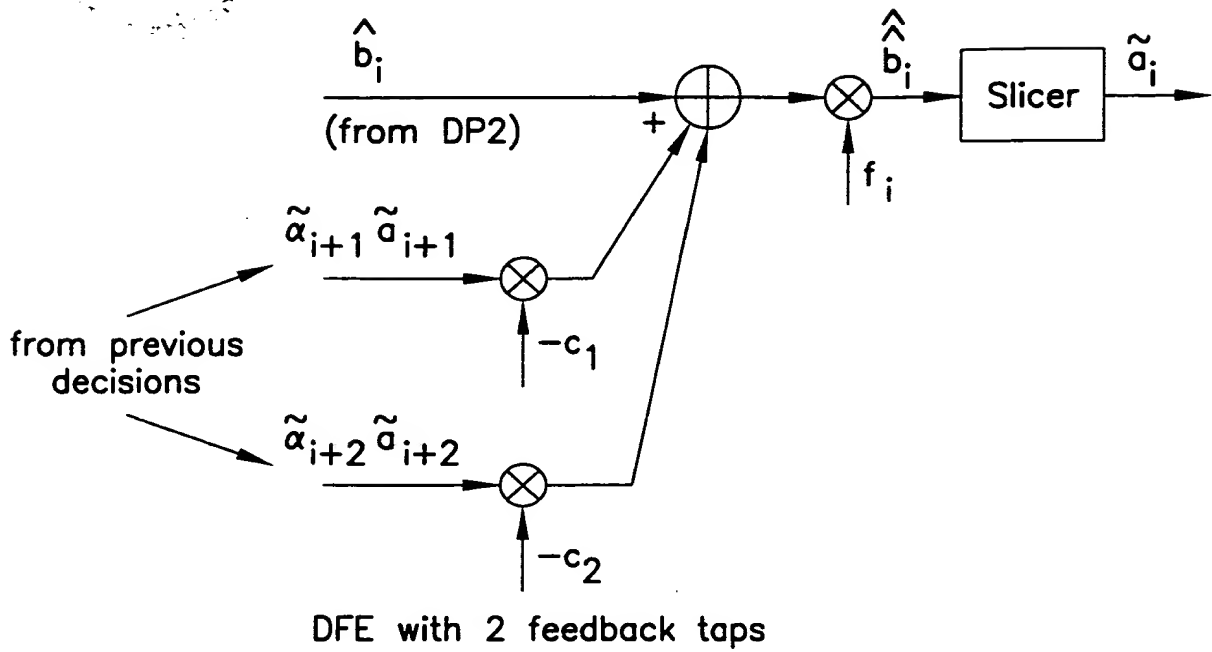
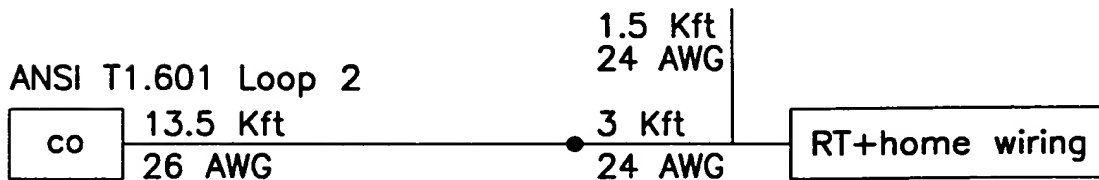


Fig. 4

Long Loop



Medium Loop

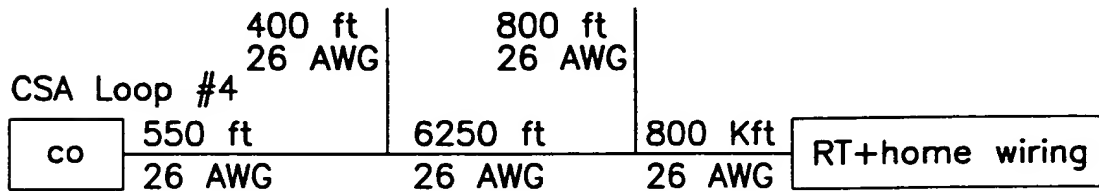
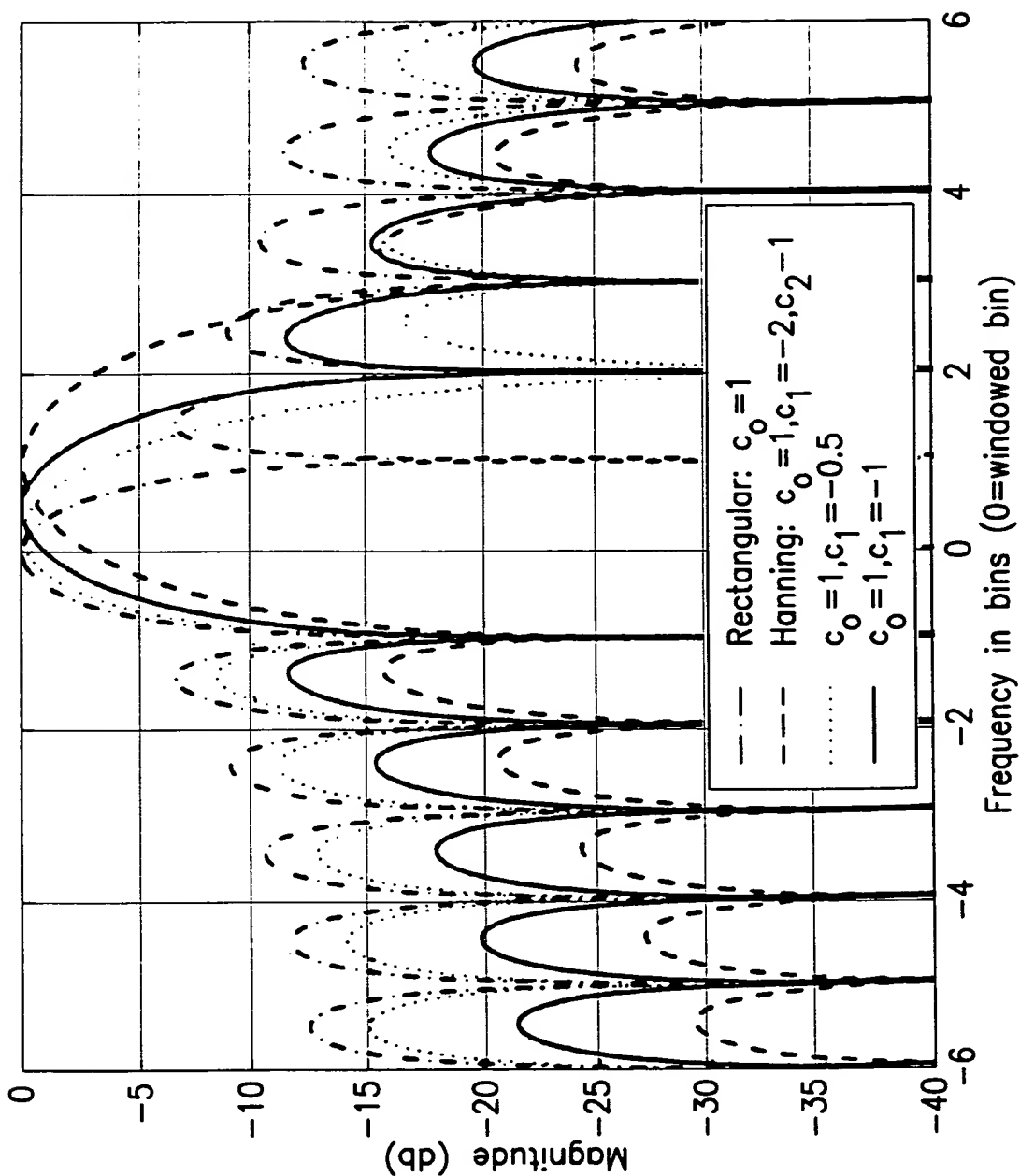


Fig. 6

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Different FDW Magnitude Responses

Fig. 5

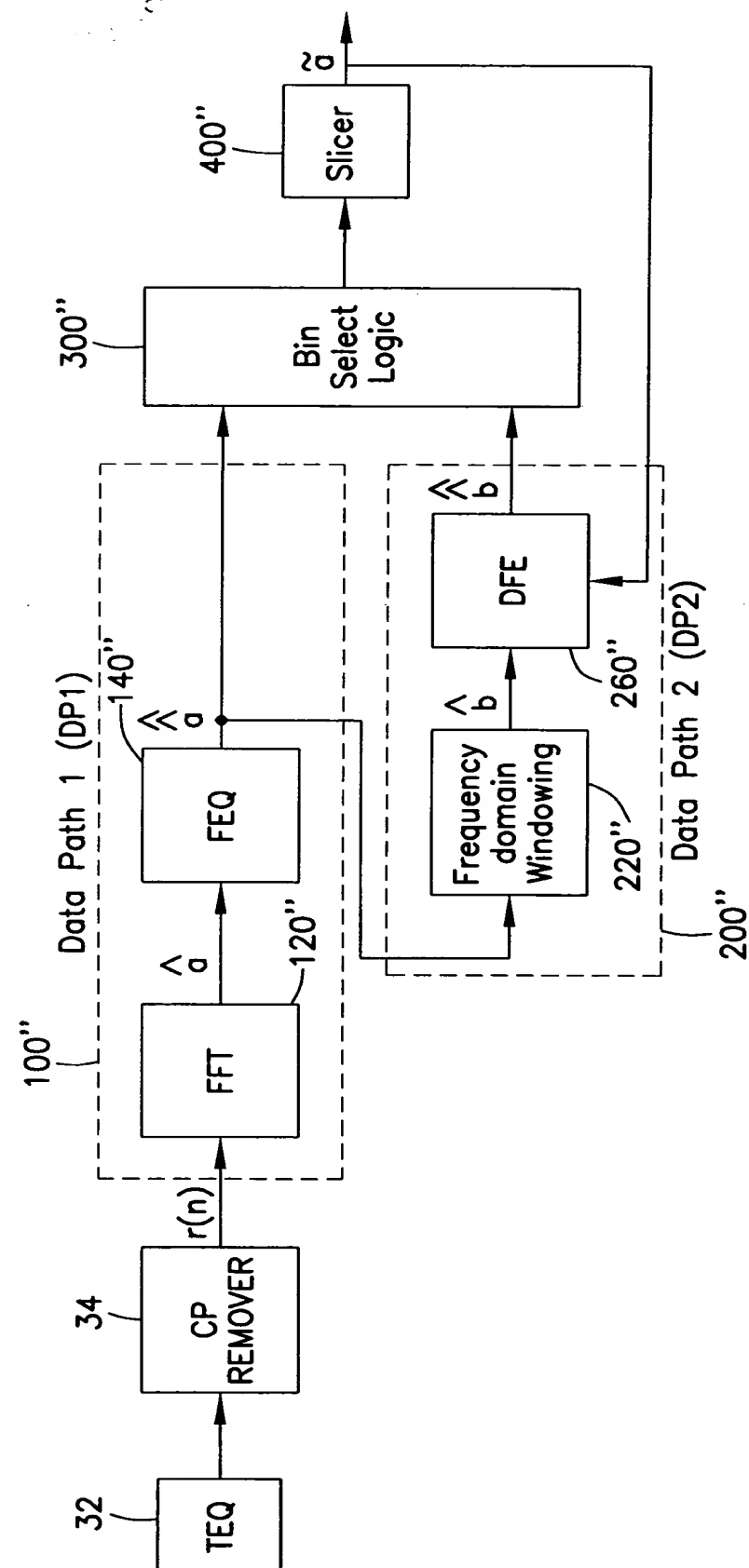
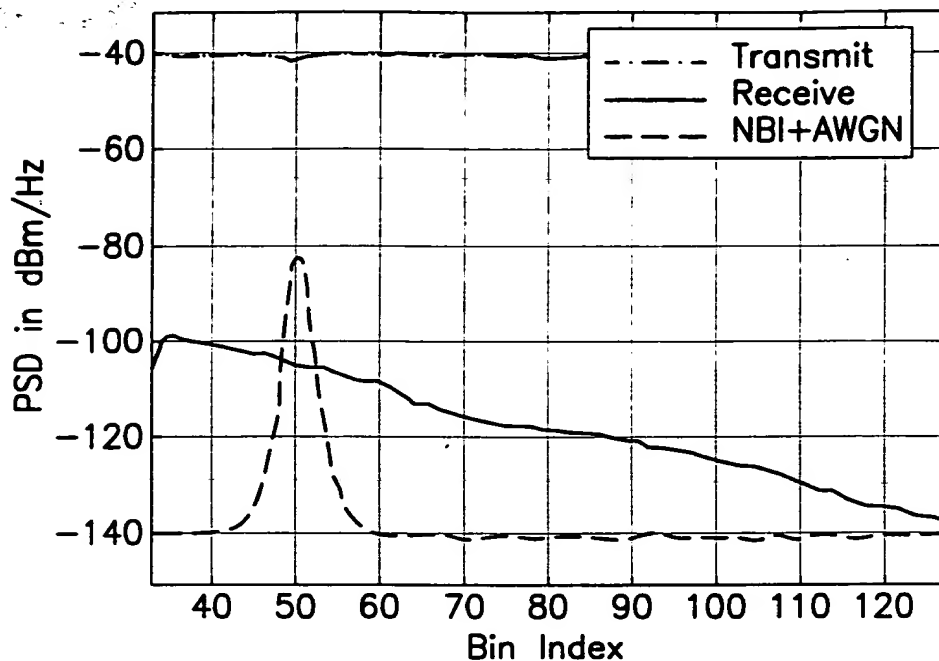


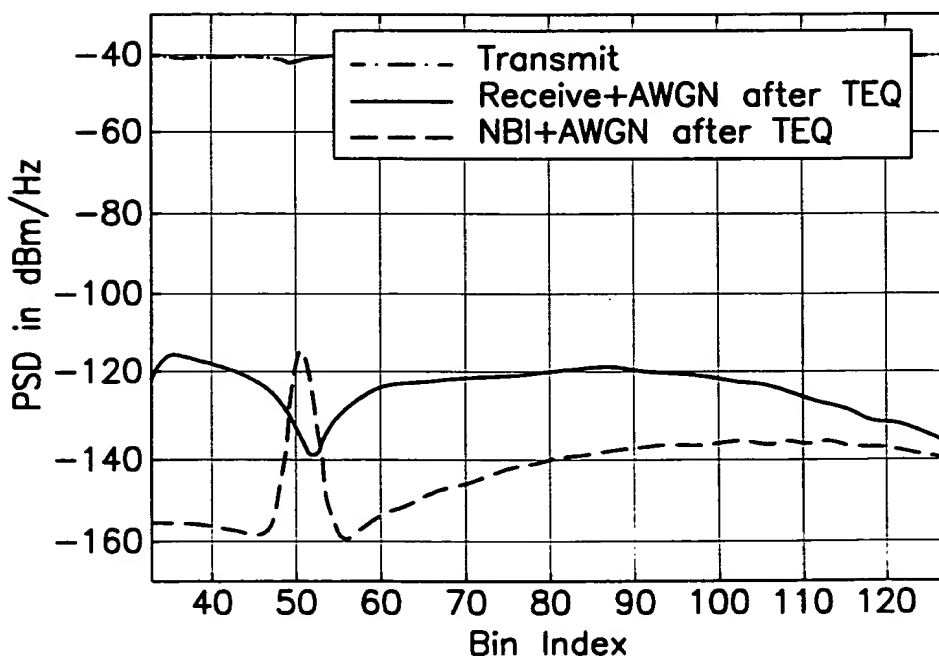
Fig. 5A

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Long Loop With NBI Signal And Noise PSD'S Before TEQ

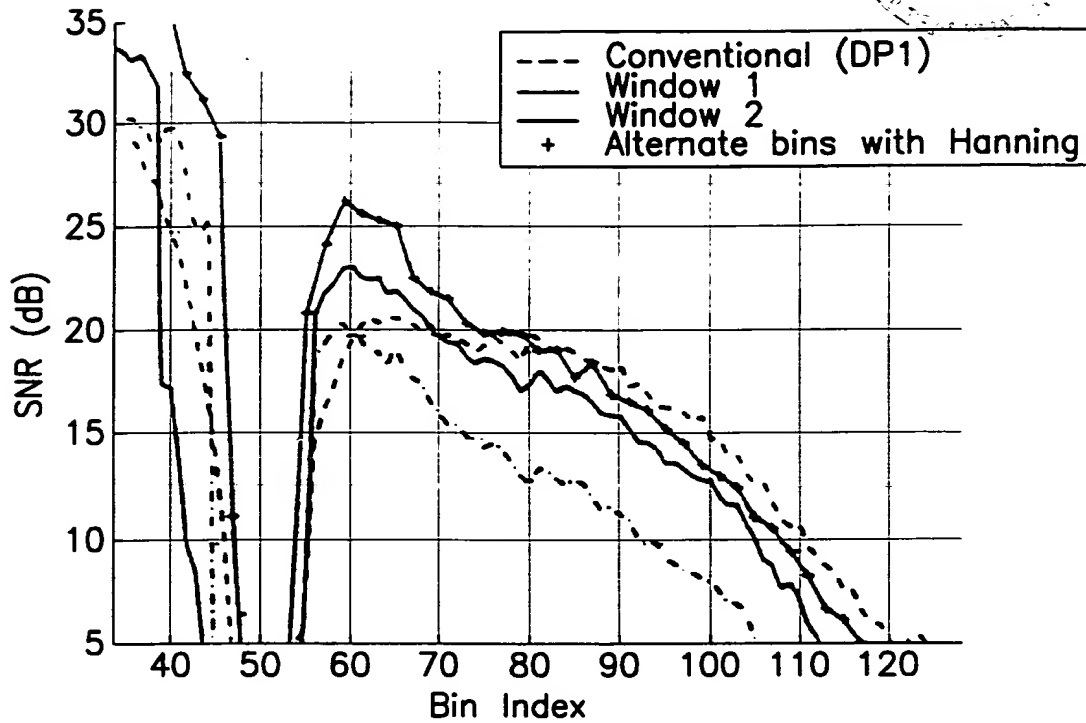
Fig. 7A



Long Loop With NBI Signal And Noise PSD'S After TEQ

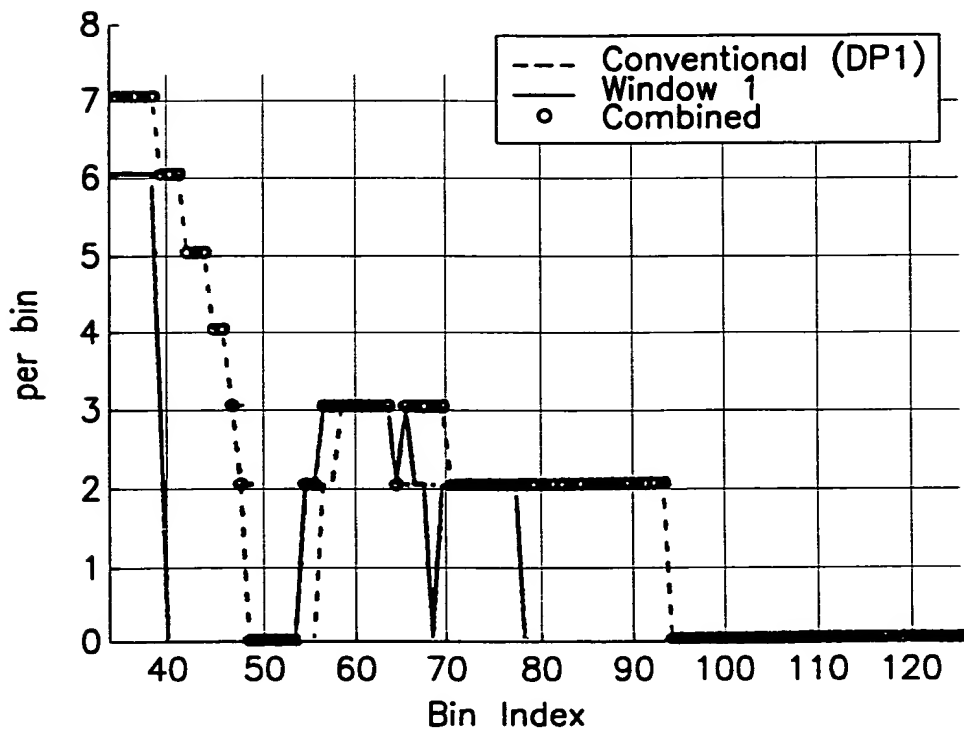
Fig. 7B

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Long Loop With NBI Profile

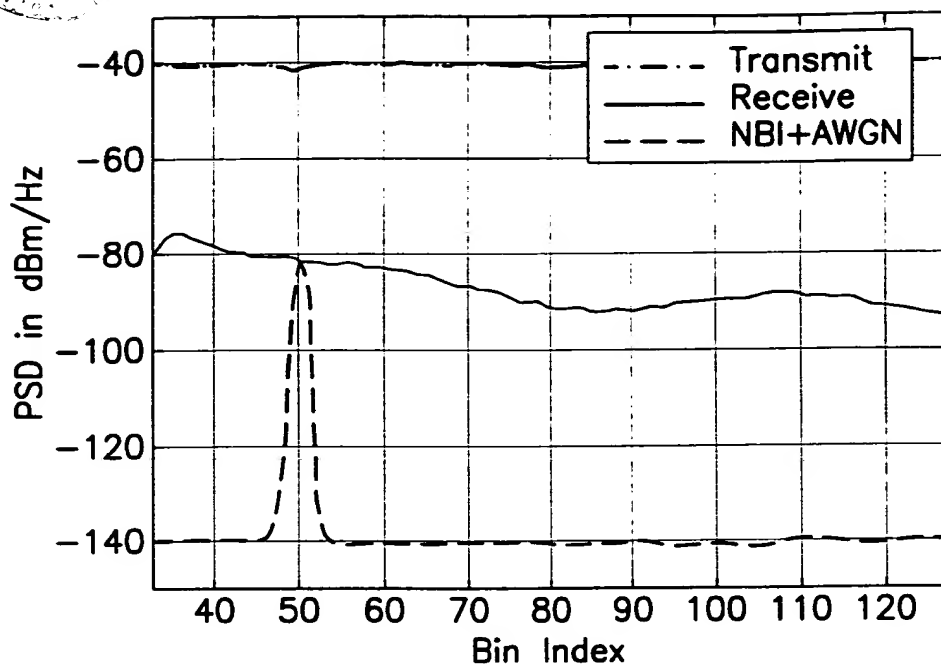
Fig. 8A



Long Loop With NBI Bit-Allocation Profile

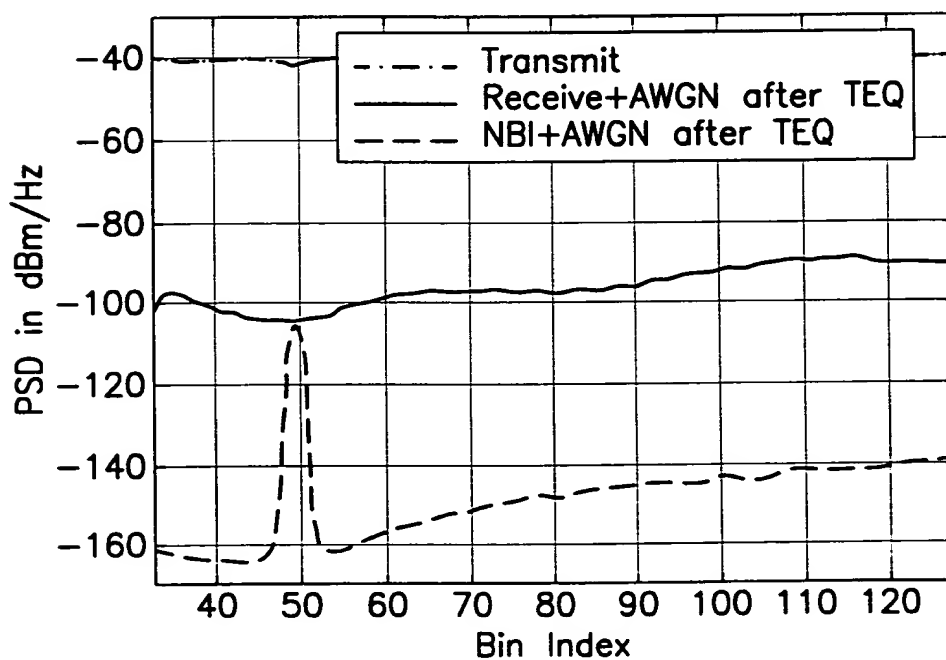
Fig. 8B

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Medium Loop with NBI Signal And Noise PSD'S Before TEQ

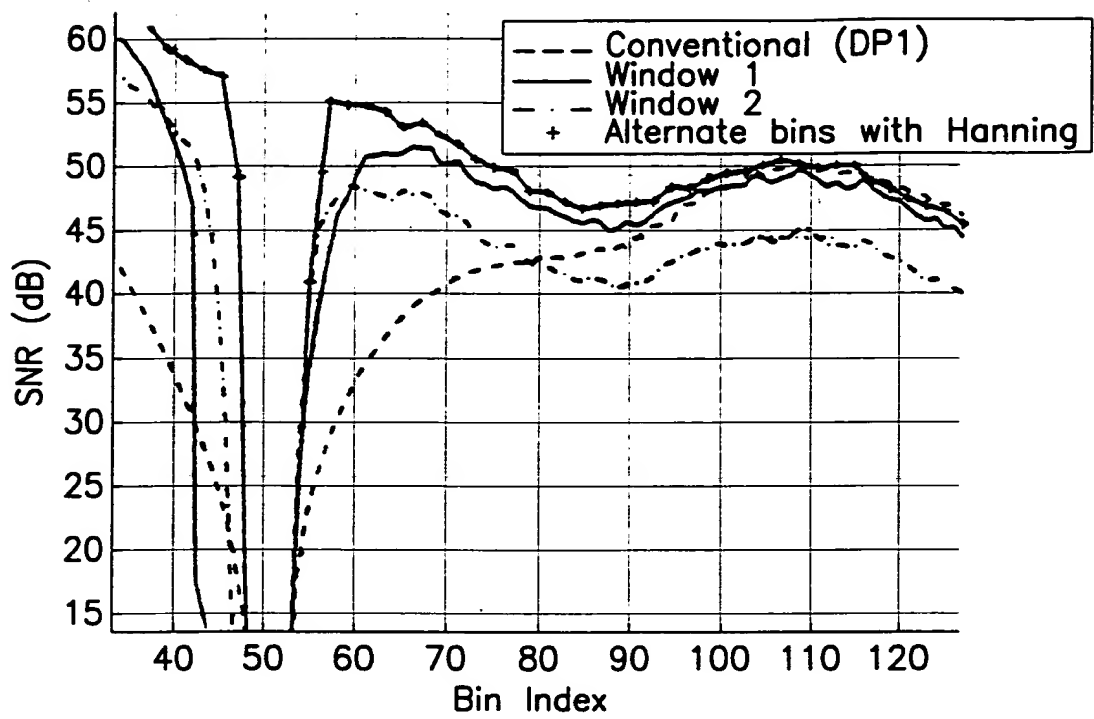
Fig. 9A



Medium Loop with NBI Signal And Noise PSD'S After TEQ

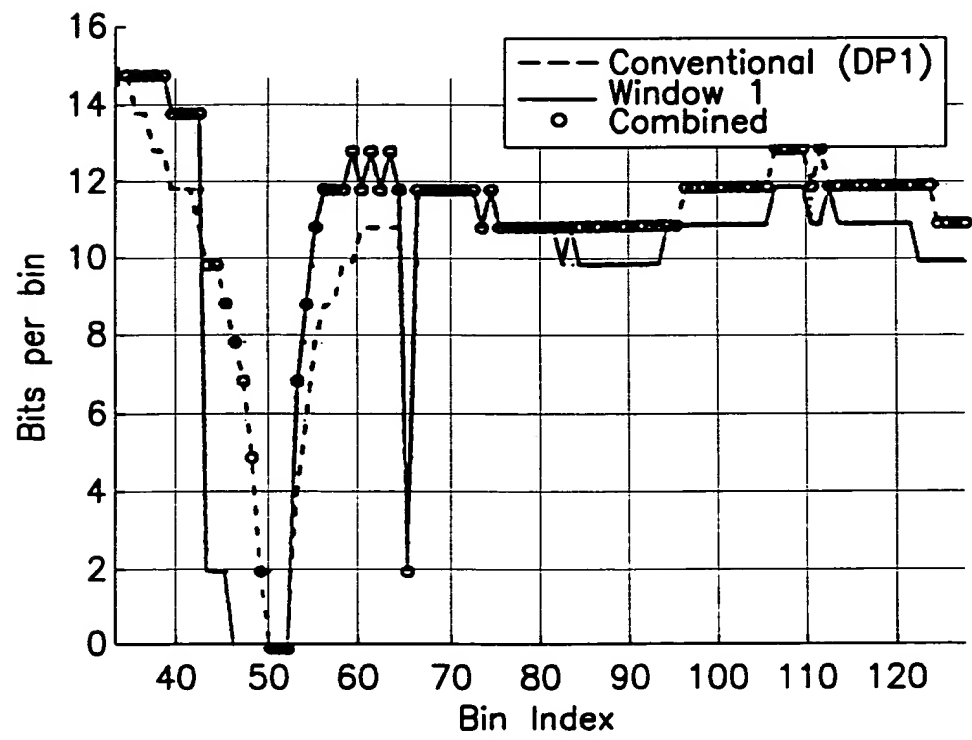
Fig. 9B

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Medium Loop With NBI SNR Profile

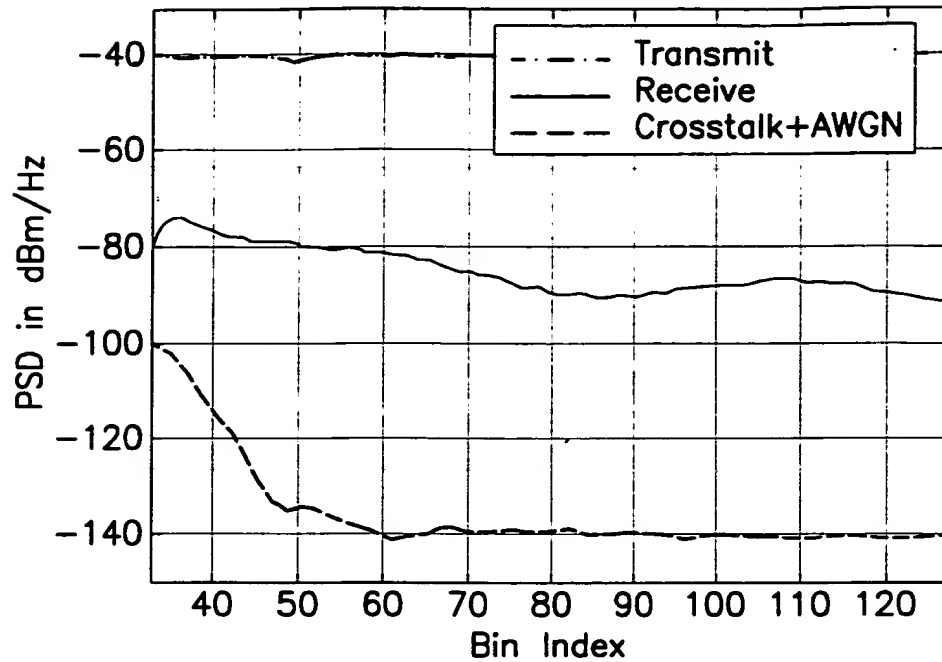
Fig. 10A



Medium Loop With NBI Bit-Allocation Profile

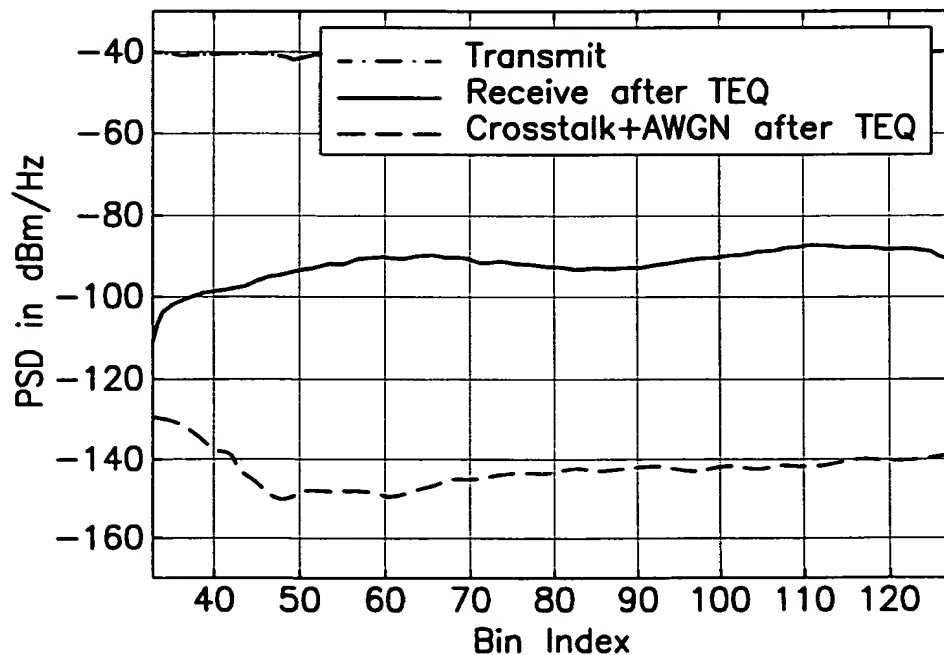
Fig. 10B

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Medium Loop With Crosstalk Signal And Noise PSD'S Before TEQ

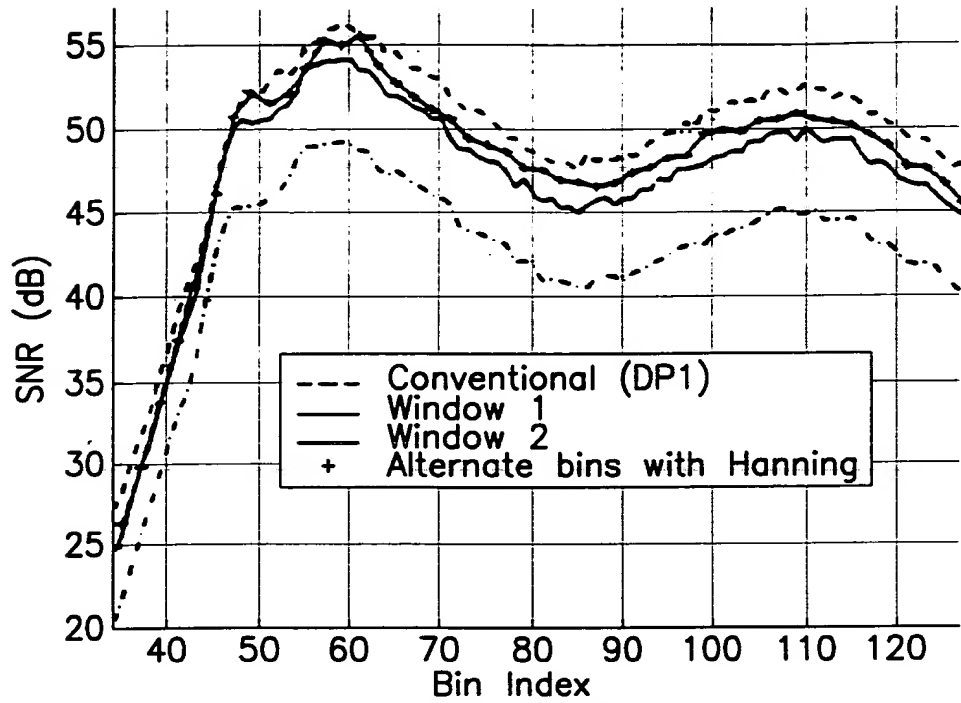
Fig. 11A



Medium Loop With Crosstalk Signal And Noise PSD'S After TEQ

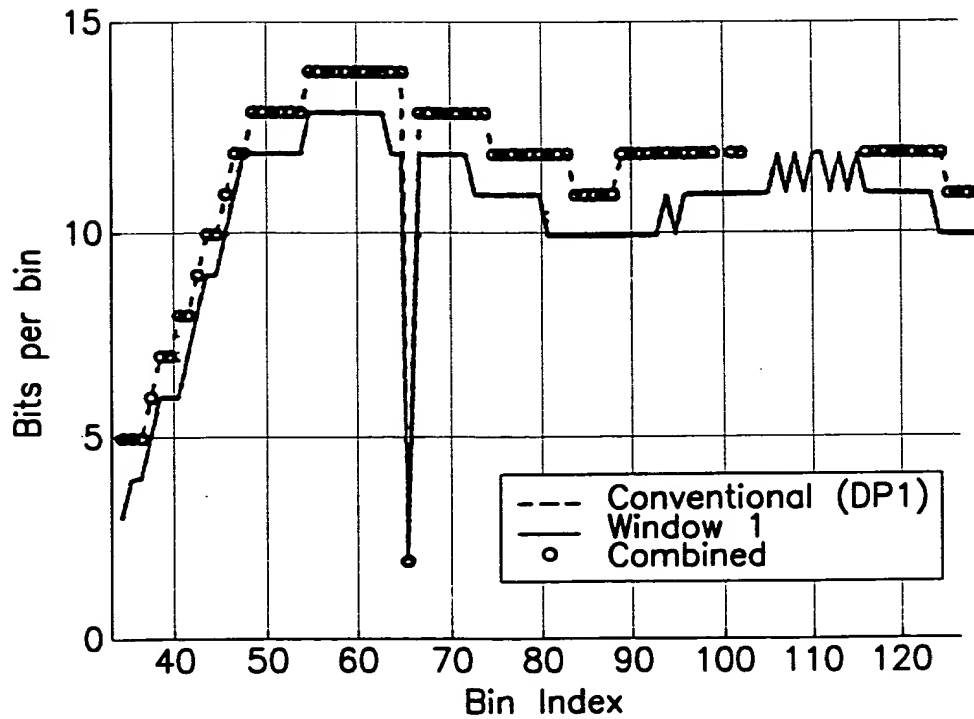
Fig. 11B

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Medium Loop With Crosstalk SNR Profile

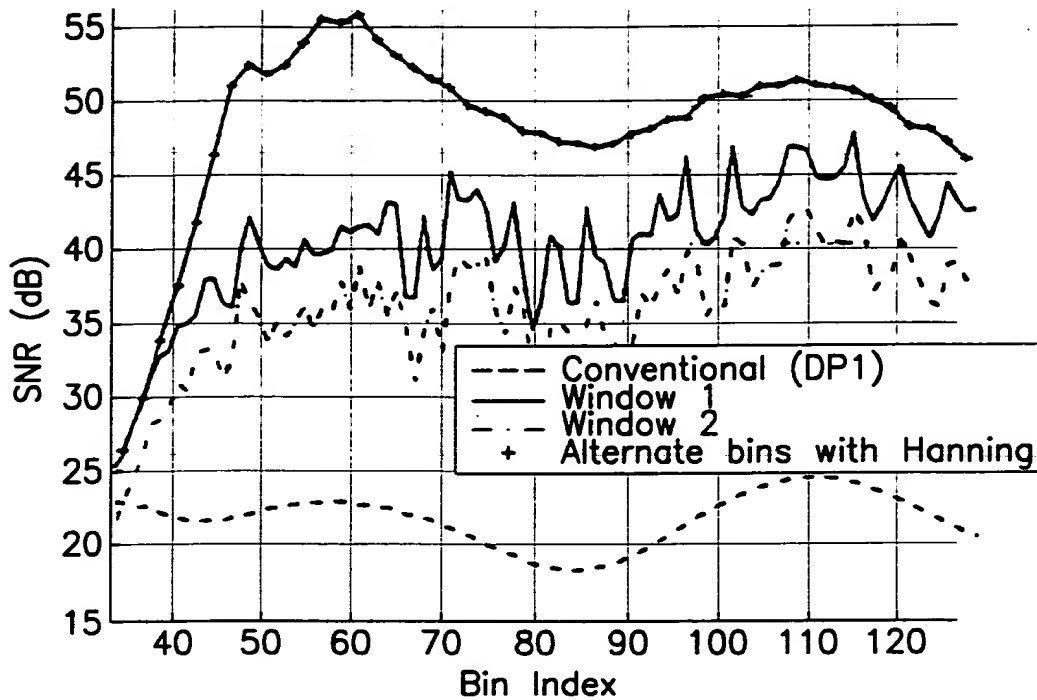
Fig. 12A



Medium Loop With Crosstalk Bit Allocation Profile

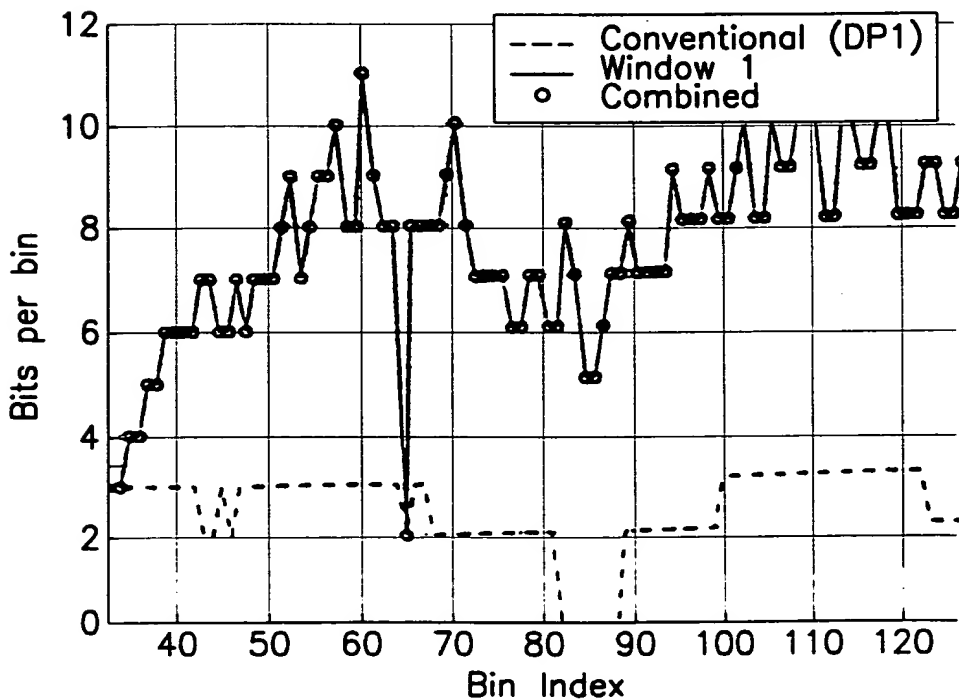
Fig. 12B

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Medium Loop With Crosstalk Without TEQ SNR Profile

Fig. 13A



Medium Loop With Crosstalk Without TEQ Bit Allocation Profile

Fig. 13B

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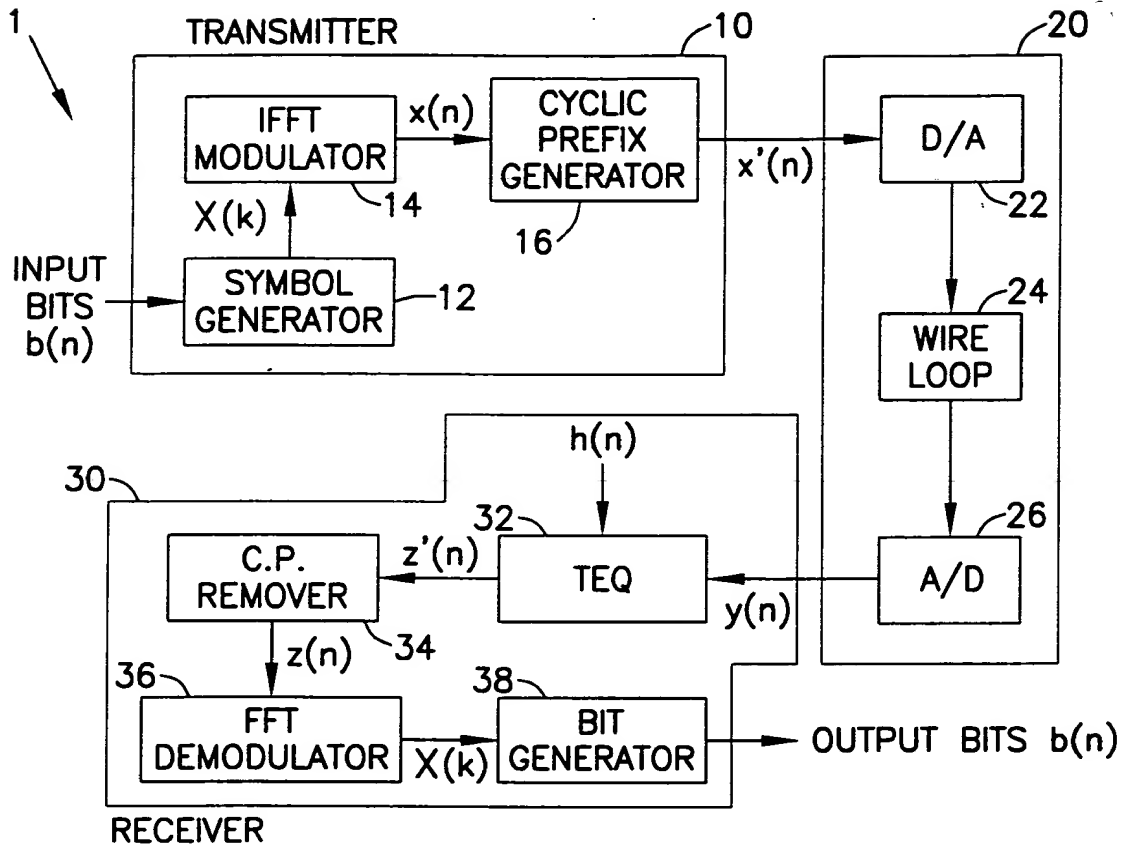


Fig. 14
 (Prior Art)

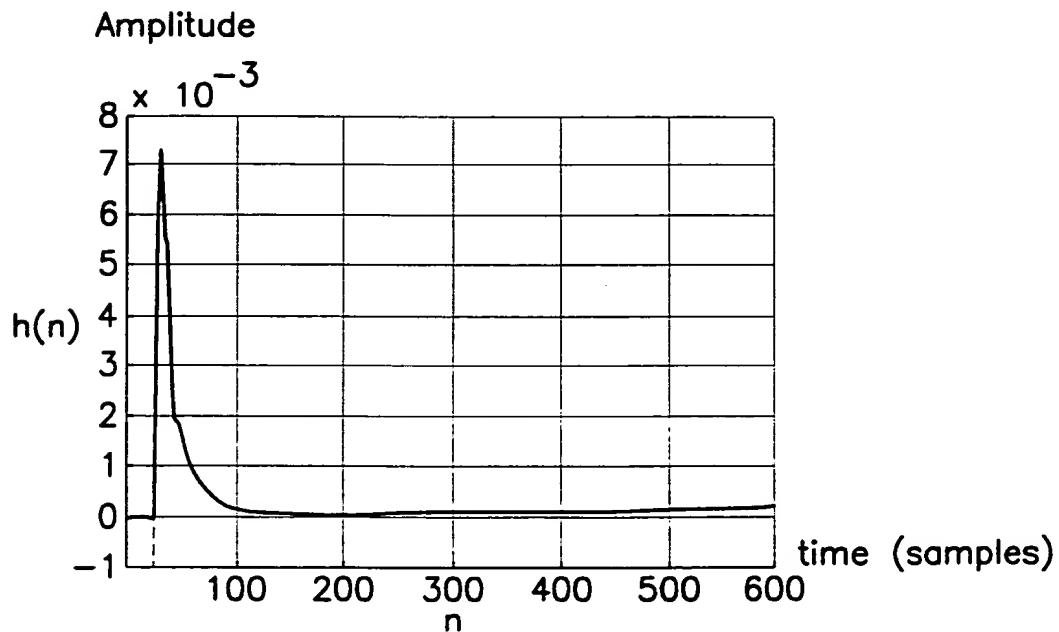


Fig. 15